EGC221: Digital Logic Lab

Experiment #8

Arithmetic Logic Unit (ALU)

Verilog Implementation

Student's Name:	Reg. no.:
Student's Name:	Reg. no.:
Semester: Spring 2017	Date: 04 April 2017

Assessment:

Assessment Point	Weight	Grade
Methodology and correctness of results		
Discussion of results		
Participation		
Assessment Points' Grade:		

Comments:

Experiment #8:

Arithmetic Logic Unit

Objectives:

The objective of this lab is:

1. To design a 4-bit ALU
2. To implement the ALU on an (Altera) FPGA Development Board
3. To verify the operation of the ALU through simulation
4. To experimentally check the operation of the ALU

In this lab, you are asked to implement the ALU using Verilog programming language. There are multiple ways you can design your circuit. The following write-up serves as a guideline to help you design the lab. However, if you find more efficient or more elegant ways to implement parts of the ALU, go ahead. Just make sure you justify your design and explain it clearly in the lab report write-up.

Pre-lab assignment:

a. Problem Statement:

An Arithmetic and Logic Unit (ALU) is a combinational circuit that performs arithmetic and logic micro-operations on a pair of n-bit operands (e.g., A[3:0] and B[3:0]). The operations performed by an ALU are controlled by a set of function-select inputs. In this lab you will design a 4-bit ALU with 3 function-select inputs: Selects: S0, S1, and Mode: M. The functions performed by the ALU are specified in Table 1.

Table 1: Functions of ALU

Logic				
M	S1	S0	FUNCTION	OPERATION (bit wise)
0	0	0	A · B	AND
0	0	1	A + B	OR
0	1	0	A $\oplus$ B	XOR
0	1	1	A’	NOT
Arithmetic				
M	S1	S0	FUNCTION	OPERATION
1	0	0	A + B	Addition
1	0	1	A - B	Subtract
1	1	0	A + 1	Increment
1	1	1	A - 1	Decrement

Besides the functions, you are required to provide status bits (flags) that indicate whether or not certain conditions have taken place following an arithmetic or logic operation. For arithmetic operations you need flags for carry (C), negative (N), zero (Z), and overflow (V) conditions. For logic operations you need the carry (C), negative (N), and zero (Z) flags.

A block diagram is given in Figure 1.

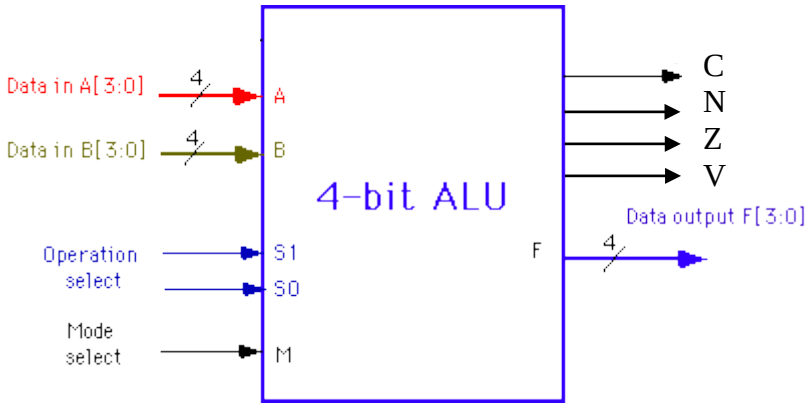

Figure 1: Block diagram of the 4-bit ALU.

b. Possible design strategies

A possible block diagram of the ALU is shown in Figure 2. It consists of three modules: 2:1 MUX, a Logic unit and an Arithmetic unit. You may employ a structural, dataflow, or behavioral model to design your circuit.

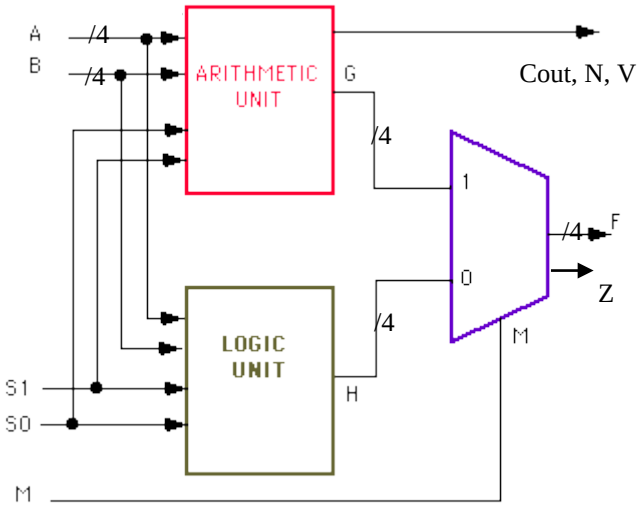

Figure 2: Block diagram of the ALU

Hand-in

Hand-in

You have to hand in a lab report that contains the following:

1. Course Title, Lab number and title, your name(s) and date (You can use the cover sheet provided with this handout.)

2. Theory of topic (ALU)

3. Section on the Pre-lab explaining the design of each macro (high-level view.)

4. Section on the lab experiment:

    a. Brief description of the goals.
    b. Brief explanation of the design approach, the overall Verilog code of each module.
    c. Verilog code for each module
    d. Logic simulations
    e. Discussion of the results indicating that the circuit functions properly.

5. Conclusion and overall discussion.

The lab report is an important part of the laboratory. Write it carefully, be clear and well organized. It is the only way to convey that you did a great job in the lab. It is necessary that you use computer tools (MS Word, Visio, Altera, etc.) to document the entire lab report.